AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (previously presented) A semiconductor device, comprising:

a bonding pad on a semiconductor substrate;

an upper copper layer on a lower surface of said bonding pad with a barrier metal interposed; and

a lower copper layer closer to said semiconductor substrate than said upper copper layer;

wherein a copper area ratio of said lower copper layer under said bonding pad is lower than that of said upper copper layer, and

wherein said lower copper layer is not electrically connected to said upper copper layer under said bonding pad.

2. (canceled)

3. (original) A semiconductor device according to claim 1, wherein the copper area ratio of said upper copper layer is greater than that of other copper layers that are formed as circuit interconnects on said semiconductor substrate.

4. (original) A semiconductor device according to claim 1, wherein the copper area ratio of said upper copper layer is at least 70%.

5. (previously presented) A semiconductor device according to claim 1, wherein the planar dimensions of said bonding pad and said upper copper layer are substantially equal.

6. (original) A semiconductor device according to claim 1, wherein said upper copper layer is constituted by a plurality of copper layers.

7. (original) A semiconductor device according to claim 6, wherein the copper area ratios of each copper layer of said upper copper layer are substantially the same.

8. (original) A semiconductor device according to claim 6, further comprising:

interlevel dielectric films that are provided between each of the copper layers of said upper copper layer; and

via-plugs composed of copper that are embedded in said interlevel dielectric films;

wherein each of the copper layers of said upper copper layer are connected by way of said via-plugs.

9. (original) A semiconductor device according to claim 8, wherein the copper layer pattern of the copper layer that is positioned uppermost in said upper copper layer and said via-plugs that are connected to the copper layer pattern are embedded in a dielectric film that is composed of a first material.

10. (original) A semiconductor device according to claim 1, wherein the copper area ratio of said lower copper layer is at least 15% and not greater than 95%.

11. (previously presented) A semiconductor device according to claim 9, wherein said lower copper layer is constituted by a plurality of copper layers.

12-13. (canceled)

14. (previously presented) A semiconductor device according to claim 11, wherein each of the copper layers of said lower copper layer are constituted by a copper pattern that is embedded in a dielectric film that is composed of a second material having a lower relative dielectric constant than said first material.

15-41. (canceled)

42. (currently amended) A semiconductor device comprising:

a bonding region in which a bonding pad is formed;

an internal circuit region provided inside of said bonding region, said internal circuit region having a multilevel wiring structure that includes a plurality of copper interconnect layers at a first level and a plurality of copper interconnect layers at second level; and

[[a]] an upper copper layer formed in said bonding region above said internal circuit region and under said bonding pad in electrical contact therewith, one of said copper interconnect layers at said first level being elongated from said internal circuit region to said bonding region under said upper copper layer in electrical isolation therefrom.

43. (currently amended) The device as claimed in claim 42, wherein one of said copper interconnect layers at said second level is further elongated from said internal circuit region to said bonding region under said upper copper layer in electrical isolation from said upper copper layer and from one of said copper interconnect layers at said first level.

44. (currently amended) The device as claimed in claim 42, wherein said upper copper layer includes first and second copper layers and a via-plug sandwiched therebetween.

45. (currently amended) The device as claimed in claim 44, ~~wherein said multilevel wiring structure~~ further ~~includes~~ comprising a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

46. (previously presented) The device as claimed in claim 45, wherein said bonding pad is in electrical contact with said second copper layer, and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

47. (currently amended) The device as claimed in claim 43, wherein said upper copper layer includes first and second copper layers and a via-plug sandwiched therebetween, and said bonding pad is in electrical contact with said second copper layer.

48. (currently amended) The device as claimed in claim 47, ~~wherein said multilevel wiring structure~~ further ~~includes~~ comprising a plurality of copper interconnect layers at a third level and a plurality of copper interconnect layers at a fourth level, said first copper layer being formed at said third level and said second copper layer being formed at said fourth level.

49. (previously presented) The device as claimed in claim 48, wherein said bonding pad is in electrical contact with said second copper layer via a barrier metal layer and one of said copper interconnect layers at said fourth level has an electrical contact with said second copper layer.

50. (new) The semiconductor device according to claim 1, wherein the upper copper layer is separated from the lower surface of said bonding pad only by the barrier metal.

51. (new) The device as claimed in claim 42, wherein said upper copper layer is separated from said bonding pad only by a layer of a barrier metal.